Appl. No. 09/829,793 Amendment and/or Response Reply to Office Action of May 8, 2003

## Amendments to the Specification

Kindly amend the Abstract that begins on page 7, at line 1, as follows:

A data processing circuit is switchable between operation in a cache mode and a cache bypass mode. In the cache bypass mode the power supply to a cache memory is switched off to reduce power consumption.

Fig.